ISSN: 0975-8585

Research Journal of Pharmaceutical, Biological and Chemical Sciences

A Survey of The Low Power Design Techniques at The Circuit Level.

Anusha N[1]*, and Sasilatha T[2].

[1]Dept. of Electronics and Communication Engineering, S.A.Engineering College,Anna University, Chennai, Tamil Nadu, 600071, India.
[2]Dept. of Electronics and Communication Engineering, Sree Sastha Institute of Engineering and Technology, Anna University, Chennai, Tamil Nadu, 600071, India

ABSTRACT

This paper deals with the survey of all the low power design techniques available for VLSI circuits. In the current trend, there is a high demand for portable devices with extensive multimedia features. Henceforth battery life has to be extended, so the need of low power circuits is mandatory. Handheld devices must possess low power devices for better performance and long run time. A review of all the low power techniques available at the circuit level is described in this paper.

Keywords: Power dissipation, Static power, Dynamic Power

Corresponding author

ISSN: 0975-8585

INTRODUCTION

Power consumption has become a primary constraint in design, along with performance, clock frequency and die size. Lower power can be achieved only by designing at all levels of abstraction: from Operating system level to Technology level. Energy reduction techniques can also be applied at all levels of the system.

Designers should use components that deploy the latest developments in low-power technology. The most effective power savings can be achieved by making the right choices at different levels of abstraction. In addition to using power-conscious hardware design techniques, it is important to save power through careful design of the operating system and application programs.

LEVELS OF LOW POWER STRATEGIES

Levels of Abstraction:

The different low power **st**rategies occur at different levels of the system from top to down levels. The different levels include the

- Operating System level,
- Software level,
- Architecture Level,
- Circuit/Logic level,
- Technology level.

The level described is a top to down level.

Fig.1 shows the different levels of abstraction. At the Operating System level the low power techniques include partitioning and power down schemes; Partitioning is a process of splitting the hard drive into different drives to allow multiple operating systems to run on the same device. In addition to partitioning, different power management techniques are incorporated at this level.

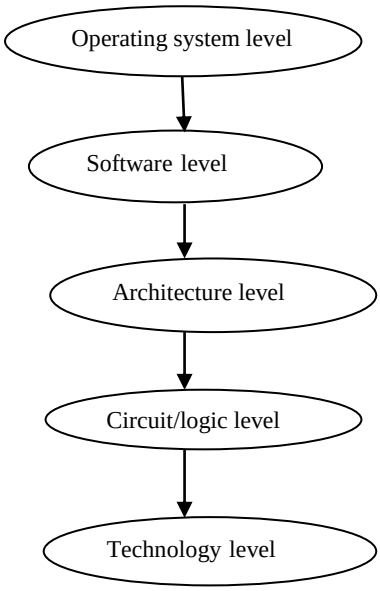

Fig.1 Levels of abstraction

In the software level of power strategies, complexity, concurrency, locality regularity, data representation reduces the power. While moving down, the architecture level implements schemes such as parallelism, pipelining, redundancy, data encoding to reduce the power. Pipelining is a process where the next instruction is fetched while current instruction is executed.Redundancy removes the data which is unused and repeated. Parallelism exhibits multitasking where multiple tasks are performed at the same time so power reduction can be achieved. The inactive modules may be turned off to save power.

In the circuit level of organization, many techniques are employed. To name a few power reduction techniques includes transistor sizing, reordering, logic optimization, activity driven power down, low swing and adiabatic switching. In the present scenario of Semiconductor industries CMOS devices have overcome the Transistor family due to its lower power consumption.CMOS family exhibits low power and still more techniques to reduce the power is incorporated of the transistors, etc. Technology level also concentrates in reduction of power by using devices with multiple thresholds. Even reduction in the threshold voltage of the device is also done.

CONCEPTS OF POWER DISSIPATION

Power dissipation is the rate of energy which is taken from the source and converted in to heat. There are 2 types of power dissipation: Static power dissipation and Dynamic Power dissipation. The former power dissipation is due to leakage current, short circuit current and bias currents. Total Power dissipated in a CMOS circuit is sum total of dynamic power, short circuit power and static or leakage power. Design for low-power implies the ability to reduce all three components of power consumption in CMOS circuits during the development of a low power electronic product.The dynamic power dissipation is due to the switching activities of transistor.

The golden equation of power dissipation is

$$P = C * V^2 * f$$

Where P is the power, C is the effective switch capacitance, V is the supply voltage, and f is the frequency of operation. For low power reduction 3 main areas include: Voltage, Physical capacitance and switching activity.

The power dissipation arises from the charging and discharging of the circuit node capacitances found on the output of every logic gate. Dynamic power dissipation also depends on the physical capacitance being switched. The capacitor can be kept as small by minimum logic, smaller devices and fewer and shorter wires. The calculation of switching activity depends on input pattern dependence, Logic function, Logic style and Circuit structure.

Every low-to-high logic transition in a digital circuit incurs a change of voltage, drawing energy from the power supply. Power dissipated is directly proportional to supply voltage and frequency. Therefore the supply voltage is scaled down then the Power dissipation decreases. On the other hand if the frequency reduces also the power dissipation also reduces. Power dissipation is also proportional to die area.

CIRCUIT LEVEL LOW POWER DESIGN TECHNIQUES

There are various low power techniques at the circuit level which is listed below

- Clock gating
- Power gating
- Transistor Sizing
- Transistor reordering
- Variable frequency
- Variable voltage supply
- Variable device threshold.

ISSN: 0975-8585

Clock Gating

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. When the system or circuit is idle supply of clock to it wastes power, So as to overcome this, clock gating techniques is employed. This gate allows the clock to propagate to the circuit only when it is required. In sequential circuits such as flip flop clock gating means disabling the clock signal when the input data does not make changes in the stored data. There are different types of clock gating schemes available which is described as follows

- AND gate based
- Latch based technique
- Flip flop based clock gating
- MUX based clock

AND gate based

AND gate produces a Logic High output only if all the inputs are high. If any one of the inputs is low, the output is also low .Using the above logic the clock signal is given as one input and enable signal as the other input. Clock propagates to the output only if the enable signal is high. The disadvantage of this method is that it results in hazards, when enable signal goes on and off multiple times. It is shown in the Fig 2.

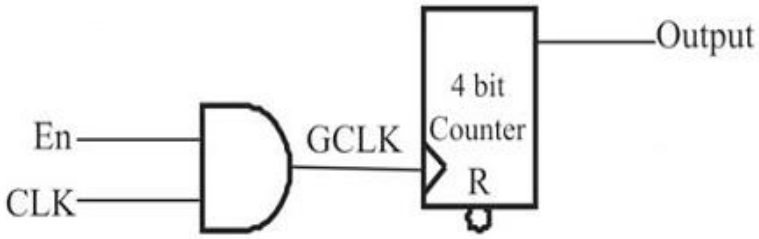

Fig.2 AND based technique

Latch Based Technique:

It is transparent that AND gate techniques results in hazards so as to overcome this edge sensitive latch is used for clock gating. The latch based clock gating style adds a level-sensitive latch to the design to hold the enable signal from the active edge of the clock until the inactive edge of the clock. Hazard are eliminated but unwanted switching transient called as glitches occur due to the propagation delays.Fig.3 shows an example of latch based technique.

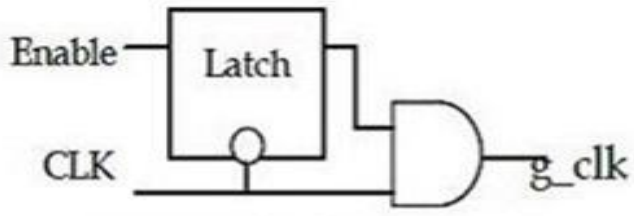

Fig.3 Latch based techniques

ISSN: 0975-8585

Flip Flop Based Clock Gating:

In this method instead of latch, D flip flop is used. The probability of missing the change on the enable pin is high due to longer sleep period. Hence forth this method is not preferable. Fig 4 shows the flip flop based clock gating.

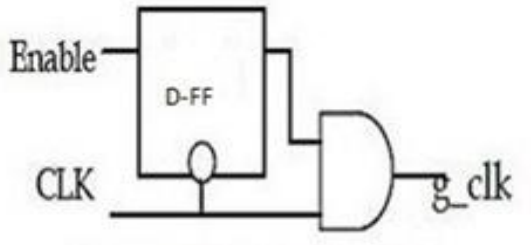

Fig.4 Flip flop based clock gating

MUX Based Clock Gating:

Multiplexer is a many to one combinational circuit. Many inputs are transferred to the single output line using the select lines. The feedback path is controlled by the MUX and MUX is controlled by the MUX select line when it is required to close or open the feedback path. This method consumes more power.

Limitations Of Clock Gating:

1. The main problem is the timing of the clock signal and the ability to group latches with identical gating conditions.
2. Sometimes it is difficult to reach the timing closure if the clock gating signal have larger fan out and it is driving many clocks if the latch group is very large.
3. It also does not consider the possibility of one part of the functional unit is in use while the other is not in use.
4. In traditional clock gating, it does not take into account the switching activities of the registers it involves.
5. Clock gating reduces test-coverage of the circuit because clock gated registers are not clocked until the enable signal is high

POWER Gating

Power gating is a technique for to reduce the power consumption by switching off the supply voltage to the circuit blocks which is idle. This technique reduces the static power dissipation because the block which remains idle is disconnected from the supply voltage. The architecture gets affected more than clock gating.

In the standby mode a high V_{th} sleep transistor is added between supply voltages and ground. In the standby mode to remove the leakage path the device is turned off. To switch off the blocks for small period of time internal power gating is more suitable.

Fig.5 shows the power gating methods and its working principles is as follows , Low-leakage PMOS transistors are used as header switches to shut off power supplies , the Power Gating parts of a design in the mode of sleep or standby. NMOS footer switches can also be used as sleep transistors in the design of power gating technique. The sleep transistors can be inserting to splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be

turned off. By using of cell- or cluster-based (or fine grain) approaches or distributed coarse-grained approaches Power Gating can be implemented.

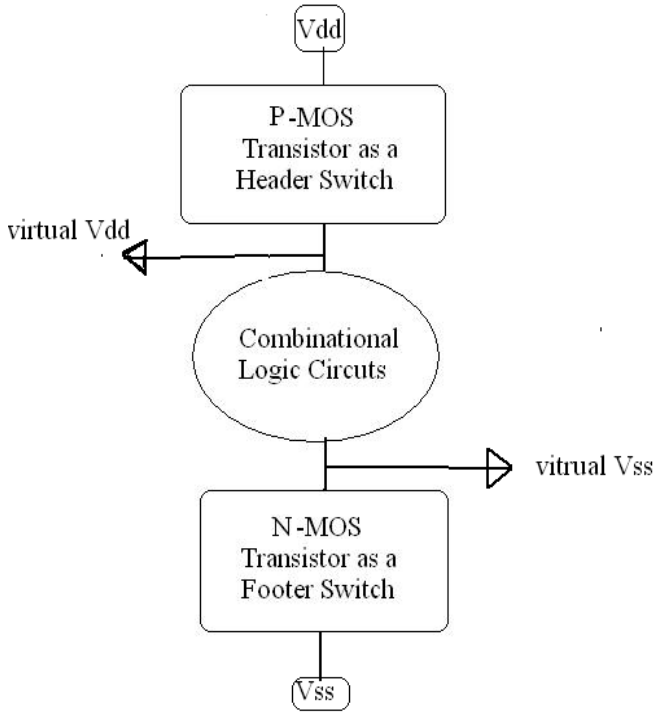

FIG.5 POWER GATING METHODS

The following is the list of parameters to be considered for power gating

- Size of the power gate
- Slew rate
- Switching capacitance
- Leakage of the power gate

***Size of the power gate*:**

The power gate must be able to handle the switching current at any time. As Rule of thumb the gate size should be 3 times the switching capacitance.

***Slew Rate**:*

Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed as volts per second. Limitations in slew rate capability can give rise to non-linear effects in electronic amplifiers. To calculate the power gating efficiency slew rate is an important factor and when slew rate is large it affects the efficiency.

***Switching capacitance**:*

If the circuit switches at a faster rate it affects the power gating efficiency.Hence the switching capacitance change should be taken in to consideration.

ISSN: 0975-8585

Leakage of Power gate:

Active transistors are used to design power gating circuits hence as active transistors will have more leakage, this parameter has to be reduced for better working of power gating circuits.

Power Gating Methods:

The Power gating methods include :***Fine grain power gating and Coarse grain power gating.***

Fine Grain Power Gating:

Each Block which is to be turned OFF has to be associated with a SLEEP transistor. On doing so increases the area,timing issues and complexity of the circuit. Fine-grain power gating encapsulates the switching transistor as a part of the standard cell logic. Switching transistors are designed by either the library IP vendor or standard cell designer. Usually these cell designs conform to the normal standard cell rules and can easily be handled by EDA tools for implementation. Fig 6 shows the Fine Grain Power Gating.

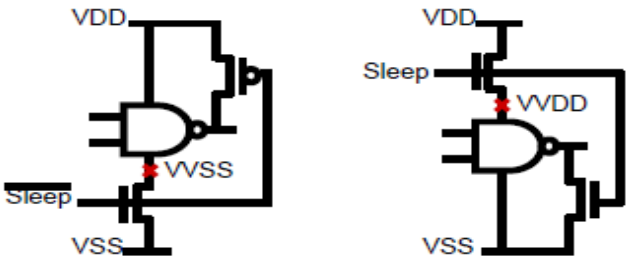

Fig.6 Fine grain power gating

Coarse Grain Power Gating:

In this method all sleep transistors are connected together between permanent power supply and virtual power supply. When compared with fine grain architecture area overhead is reduced and also charging and discharging of sleep transistors are shared between them hence PVT variations are reduced. Fig 7 shows the Coarse Grain Power Gating.

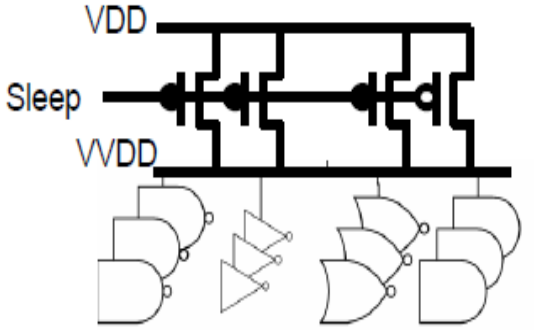

Fig.7 Coarse grain power gating

ISSN: 0975-8585

The sleep transistors are implemented in the Following configurations

1. Grid style sleep transistors
2. Ring style sleep transistors.

Fig.8 shows the ring style sleep transistors. In the ring style implementation, a virtual power ring is added to surround each power domain. The sleep transistors are placed between permanent power ring and virtual power rings to control power supply to each power domain.

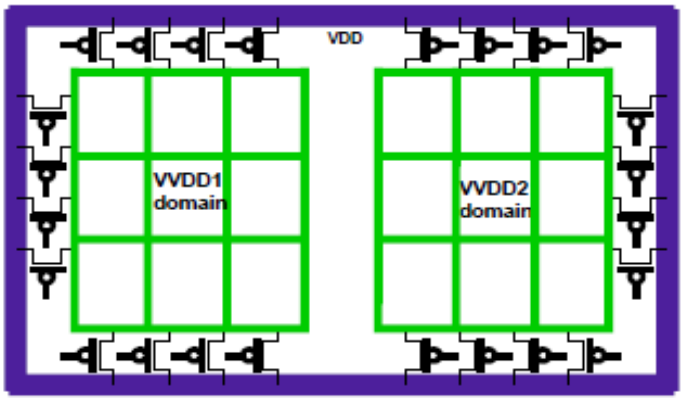

Fig.8 Ring style sleep transistors

In Fig.9 the grid style sleep transistor implementation, the sleep transistors are placed close to power grid to connect permanent power network and virtual power networks, as shown in Fig. 4. The advantages of the grid style implementation are the better IR-drop management because each sleep transistor drives local cells. The sleep transistor distribution can be optimized to consume fewer sleep transistors than in the ring style implementation on a same IR-drop target.

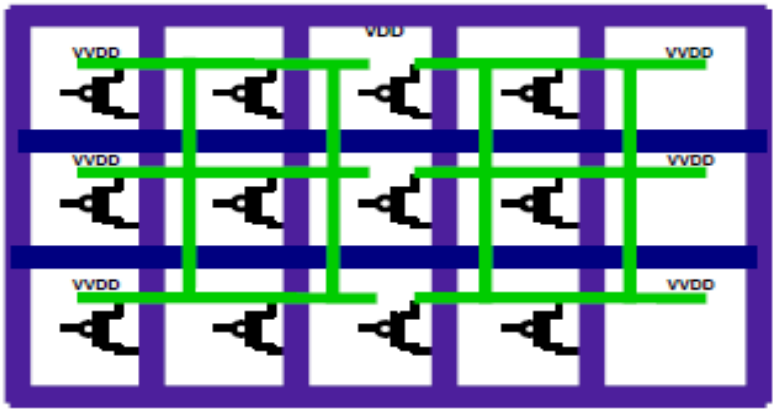

Fig.9 Grid style sleep transistor

The drawback of the implementation is its impact on routing and physical synthesis, because the sleep transistors are distributed in the design area and their placement and routing constraints restrict layout optimization and net routing.

ISSN: 0975-8585

TRANSISTOR RESIZING

Downsizing of the gates along the fast paths is done, which in turn reduces the input capacitances. This reduces the propagation delay and enhances the speed. Power dissipation is reduced by both switching and capacitance reduction. Resizing does not imply on downsizing alone even upsizing can be implemented. resizing is a complex optimization problem involving a tradeoff between output switching powers and internal short-circuits power on several gates at the same time.

TRANSISTOR REORDERING

In this method the relative difference between the best and worst propagation delays of CMOS gate is calculated by changing the order of the transistors. This method is implemented so as to reduce the propagation delay which in turn reduces the power dissipation.

VARIABLE SUPPLY VOLTAGE

Switching and short circuit power are proportional to the square of the supply voltage. • But the delay is proportional to the supply voltage. So, the decrease in supply voltage will results in slower system.

VARIABLE FREQUENCY

The golden equation of VLSI is $P = C * V^2 * f$.So if frequency is reduced the power dissipation reduces automatically.

VARIABLE DEVICE THRESHOLD

Threshold voltage is one of the most important parameters for device and as well as circuit design. The criteria for choosing the threshold voltage is as follows: Low threshold voltage foe higher performance and high threshold for reduction of leakage power. Threshold voltage can be scaled down to get the same performance, but it may increase the concern about the leakage current and noise s margin.

Moreover different threshold voltages can be used and it is called as multiple threshold devices. The various multiple threshold techniques are as follows:

- SATS – Self ADJUSTING threshold voltage scheme
- MTCMOS-Multiple threshold voltage CMOS
- DTMOS- Dynamic threshold voltage MOSFET. DGDT –SOI- double gate dynamic threshold control

The section below describes the various multiple threshold schemes:

***SATS*:**

A leakage sensor senses the leakage current and outputs a control signal to self sub bias (SSB) circuit. When there is an increase in leakage current than a certain value then the self sub bias (SSB) will be triggered which in turn reduces the substrate bias of all the other transistors.

MTCMOS:

This scheme uses both high and low threshold voltage in a single chip and a sleep control scheme is introduced for low power design.

***DTCMOS*:**

In this method gate and substrate of transistors are tied together. Because of the body effect the threshold voltage can be changed dynamically during different mode of operation. When the input is low PMOS is ON and when the input is high NMOS is ON. In the active mode the circuit switches from low to high

with a higher speed because of low Vth PMOS. In the standby mode the static leakage is decided by the sub threshold current of the high Vth NMOS and is smaller. When the IN is high the situation is just opposite. The supply voltage of DTMOS is limited by the diode built in potential. The PN junction diode between the source and body should not be forward biased. So this technique is only suitable for ultra low voltage circuits.

DGDT- SOI:

Thin film make fully depleted (FD) soi mos devices have nearly ideal sub threshold slope and small parasitic capacitance which makes it attractive in low voltage high performance applications. The threshold voltages of FD SOI devices are difficult to control. At this point back gate is used to control the front gate threshold and reduce the sensitivity of threshold voltage.

CONCLUSION

This survey paper deals with introduction about the different types of power reduction at different levels. It also describes the different methods of power reduction available at the circuit level. These techniques can be carried out to achieve low power.

REFERENCES

[1] Himanshu Chaudhary, Nitish Goyal, Nagendra Sah “Dynamic Power Reduction Using Clock Gating: A Review”, International Journal of Electronics & Communication Technology Vol.6, No.1 March 2015.

[2] Akhila Abba, K Amarender “Improved Power Gating Technique for Leakage Power Reduction “International Journal Of Engineering And Science Vol.4, Issue 10 October2014, PP 06-10 .

[3] Kaushik Roy “Low power VLSI design”.